**REMARKS**

Claims 1-20 remain in this application. No claims have been cancelled. Claims 1, 11 and 17 have been amended.

Applicants thank the Examiner for the detailed study of the application and prior art.

At the outset, Applicants note that the present claimed invention and the cited U.S. Patent No. 5,585,763 to Navabi et al. (hereinafter "Navabi") both disclose an amplifier with some controlled output impedance using feedback. There is a key distinguishment between the present claimed invention as now set forth in this Amendment and Navabi.

In the present claimed invention, the synthetic impedance driver circuit includes an input and output port and an operational amplifier having an input coupled to the input port and a single output. This single output is operatively coupled to the output port, and over a circuit path through which an output impedance of the driver circuit is synthesized with the circuit path being exclusive of one or more series-coupled electrical energy-dissipative elements so that the synthesized output impedance of the driver circuit is defined essentially exclusive of the series-coupled electrical energy-dissipative elements.

In the present invention, the single output of the operational amplifier is connected to a level shifter 71, having first and second level-shifted outputs 72 and 73. These outputs can be coupled to first and second complimentary polarity transistor circuits 80, 90, which could include current mirror transistors. Four different embodiments are shown in FIGS. 5-8, but all include the single output

operational amplifier, the level shifter, first and second level-shifted outputs and the first and second complimentary polarity transistor circuits with the current mirror circuit.

The first embodiment shown in FIG. 5 is a single end implementation that includes drivers to be coupled in a bridge configuration.

FIG. 6 shows a second embodiment with an input resistor 54 of FIG. 5 removed, but the input Vin applied to a non-inverting input of the operational amplifier.

In the third embodiment shown in FIG. 7, a load impedance can be compensated by inserting a first auxiliary resistor in the mirrored current feedback path and coupling the current mirror node 84 through a second auxiliary resistor 87.

FIG. 8 is a fourth embodiment where the current mirror node 84 tracks the output voltage at the output current node 83 and removes current mirror distortion for all values of a load resistance.

These four embodiments have in common the operational amplifier with a single output, operative in combination with the unique circuit having the single output that connects into the circuit path through which an output impedance of the driver circuit is synthesized. The circuit path is exclusive of one or more series-coupled electrical energy-dissipative elements, so that the synthesized output impedance of the driver circuit is defined essentially exclusive of the series-coupled electrical energy-dissipative elements.

Navabi shows a controlled output impedance that uses current and voltage feedback to set gain and output impedance.

A differential input gain block is formed as an internal, fully differential input amplifier that has two voltage outputs. With Navabi, a first voltage output 315 controls two P-channel output devices that are capable of sourcing currents. The second voltage output 320 controls two N-channel output devices that are capable of sinking currents. The two outputs are linked by biasing to maintain quiescent current in the output. This is further explained in column 3, starting at line 30, and continuing to the top of column 4. The two outputs are necessary for operation of the operational amplifier circuit design in Navabi.

It is thus clear that Navabi teaches opposite from the claimed invention, which uses a single output that is connected through the circuit path to the single output port.

Accordingly, Applicants contend that the present case is in condition for allowance and respectfully requests that the Examiner issue a Notice of Allowance and Issue Fee Due. If the Examiner has any questions or suggestions for placing this case in condition for allowance, the undersigned attorney would appreciate a telephone call.

Respectfully submitted,

RICHARD K. WARTHER
Reg. No. 32,180
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
Phone: 407-841-2330

In re Patent Application of:
**JOFFE ET AL.**
Serial No. **09/997,228**
Filing Date: **11/29/01**

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: **MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450**, on this 31st day of August, 2004.

Julie Lalan